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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NG, CHRISTINE Y	
ART UNIT	**PAPER NUMBER**
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/044,625	JONES, DELON K.	
	Examiner	Art Unit	
	Christine Ng	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4, 7-10, 12, 13, 15 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,411,143 to Fernandez-Texon in view of U.S. Publication No. 2002/0080825 to Wolf et al.

Referring to claim 1 and 12, Fernandez-Texon disclose in Figure 1A a multiple access communication system comprising:

Master sector equipment (master PLL 12) adapted to control the overall operation of said system, and said master sector equipment comprising a master clock generator (master PLL VCO 16) adapted to generate a master clock signal (VCO clock signal 24). Refer to Column 2, line 28 to Column 3, line 3.

Slave sector equipment (slave PLL 14) adapted to transmit and receive communications directly to and from Customer Premises Equipment (CPE) in the system. Refer to Column 2, line 28 to Column 3, line 3.

For each of the slave sector equipment, a cable (line connecting master PLL 12 with slave PLL 14) coupled between it and said master sector equipment for transmitting and receiving signals including said master clock signal. Refer to Column 2, line 28 to Column 3, line 3.

Each of the slave sector equipment comprising a PLL (slave PLL 14) receiving at an input (input divider 34), said master clock signal, and allowing a phase (VCO clock signal 36) to be chosen. Refer to Column 2, line 28 to Column 3, line 3.

Nonvolatile memory (in slave PLL VCO 16) adapted to store for each of the slave sector equipment, the appropriate phase. Slave PLL VCO 16 determines and stores VCO clock signal 36. Refer to Column 2, line 28 to Column 3, line 3.

Fernandez-Texon does not disclose a *plurality* of slave sector equipment.

Wolf et al disclose that in a telecommunications system, many modules (slave equipment) operate in synchronism by receiving a central clock signal from a central clock generator (master equipment). The modules then synchronize their own local clock generators with the central clock signal. Refer to Paragraph 0003. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a *plurality* of slave sector equipment. One would have been motivated to do so since a system generally has several nodes that need to communicate with each other, so synchronization is necessary in order for data transmission.

Fernandez-Texon does not disclose that each of the slave sector equipment comprises a programmable, multiple tap slave sector PLL; a "phase select" tap is chosen so that said slave sector PLL outputs a slave sector clock signal which matches within a predefined tolerance, the phase delay of the slave sector clock signal of the slave sector equipment having the longest cable coupled thereto; and that the nonvolatile memory is adapted to store the appropriate "phase select" tap to satisfy the predefined delay matching tolerance.

Wolf et al disclose in Figure 1 a network device that is used to synchronize to a master clock. The network device uses a PLL to choose a master clock signal between two incoming clock signals TS1,TS2. Clock signals TS1, TS2 are redundant clock signals with different phases, one of which is chosen ("phase select") as the master synchronization signal by compensation modules MOD1,MOD2 (Paragraph 0038). The clock signals TS1, TS2 may be arriving on different length cables, so MOD1,MOD2 can choose the clock signal from the longest cable (Paragraph 0032) while accounting for a predetermined tolerance (Paragraph 0028). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that each of the slave sector equipment comprises a programmable, multiple tap slave sector PLL; a "phase select" tap is chosen so that said slave sector PLL outputs a slave sector clock signal which matches within a predefined tolerance, the phase delay of the slave sector clock signal of the slave sector equipment having the longest cable coupled thereto; and that the nonvolatile memory is adapted to store the appropriate "phase select" tap to satisfy the predefined delay matching tolerance. One would have been motivated to do so in order to so since longer cables will cause a greater signal delay and transmission time. By adjusting the clock signal to the longest cable, the system can accommodate for the worst case signal delay and transmission time. Refer to Paragraphs 0004 and 0032.

Referring to claims 2 and 13, Fernandez-Texon disclose in Figure 1A wherein said nonvolatile memory (slave PLL VCO 16) is distributed and self-contained among each of the slave sector equipment. Refer to Column 2, line 28 to Column 3, line 3.

Referring to claims 4 and 15, refer to the rejection of claims 1 and 12. Fernanedez-Toxen disclose in Figure 1A that the master PLL 12 and slave PLL 14 have the same structure. Refer to Column 2, line 28 to Column 3, line 3.

Referring to claims 7 and 18, Fernandez-Toxen discloses in Figure 1A wherein said slave sector PLLs comprise a forward path comprising a phase comparator (slave PLL phase detector 20) and a voltage-controlled oscillator (slave PLL VCO 16); and a feedback loop (from slave PLL VCO 16) comprising clock shift circuitry (clocking adjustment from slave PLL charge pump and loop filter 18). Refer to Column 2, line 28 to Column 3, line 3.

Fernandez-Toxen does not disclose that said clock shift circuitry comprising multiple "phase select" taps.

Wolf et al disclose in Figure 1 a network device that is used to synchronize to a master clock. The network device uses a PLL to choose a master clock signal between two incoming clock signals TS1,TS2. Clock signals TS1, TS2 are redundant clock signals with different phases, one of which is chosen ("phase select") as the master synchronization signal by compensation modules MOD1,MOD2 (Paragraph 0038). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that said clock shift circuitry comprising multiple "phase select" taps. One would have been motivated to do so in order to so the node can choose between different phases.

Referring to claims 8 and 19, Fernandez-Toxen discloses in Figure 1A wherein said feedback loop further comprises a voltage-controlled oscillator frequency divider

(slave PLL loop divider). Refer to Column 2, line 28 to Column 3, line 3.

Referring to claims 9 and 20, refer to the rejection of claims 7 and 18. Fernanedez-Toxen disclose in Figure 1A that the master PLL 12 and slave PLL 14 have the same structure. Refer to Column 2, line 28 to Column 3, line 3.

Referring to claims 10 and 21, refer to the rejection of claims 8 and 19. Fernanedez-Toxen disclose in Figure 1A that the master PLL 12 and slave PLL 14 have the same structure. Refer to Column 2, line 28 to Column 3, line 3.

3. Claims 3, 5, 11, 14, 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,411,143 to Fernandez-Texon in view of U.S. Publication No. 2002/0080825 to Wolf et al, and in further view of U.S. Patent No. 6,259,901 to Shinomiya et al.

Referring to claims 3 and 14, Fernandez-Texon does not disclose wherein said slave sector PLLs are subsumed by MODEMs.

Shinomiya et al disclose in Figure 1 a telephone that includes PLL's 221,223 and modems 3r,3t . Refer to Column 5, lines 45-55. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include wherein said slave sector PLLs are subsumed by MODEMs. One would have been motivated to do so in order since modems provide for the conversion of analog signals into digital signal and digital signals into analog signals, thereby allowing analog and digital devices to communicate.

Referring to claims 5 and 16, Fernandez-Toxen does not disclose wherein said master sector PLL is subsumed by a MODEM. Refer to the rejection of claims 3 and

14. Fernanedez-Toxen disclose in Figure 1A that the master PLL 12 and slave PLL 14 have the same structure. Refer to Column 2, line 28 to Column 3, line 3.

Referring to claims 11 and 22, Fernandez-Toxen does not disclose wherein said system is adapted for synchronous Code Division Multiple Access (CDMA) communication.

Shinomiya et al a system in Figure 1 a CDMA or W-CDMA system that uses PLL's 221,223. Refer to Column 1, lines 50-59; and Column 5, lines 20-27. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include wherein said system is adapted for synchronous Code Division Multiple Access (CDMA) communication. One would have been motivated to do so since CDMA one of the multiple access technologies, thereby making the system more flexible.

4. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,411,143 to Fernandez-Texon in view of U.S. Publication No. 2002/0080825 to Wolf et al, and in further view of U.S. Patent No. 5,986,641 to Shimamoto.

Fernandez-Toxen does not disclose wherein said master sector equipment further comprises driver circuitry coupled at its outputs to said cables, and coupled at its inputs to said master sector PLL and said master clock generator, said driver circuitry adapted to boost signal levels.

Shimamoto disclose in Figure 2 a PLL 8 that has driver circuitry 13 coupled at its outputs to a connector 3. In Figure 3, a PLL 21 has driver circuitry 26 at its input. "The

PLL circuit boosts a low potential clock signal received via the fifth driver 26 and restores it to the original clock signal" (Column 6, lines 21-23). Refer also to Column 5, line 35 to Column 6, line 20. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include wherein said master sector equipment further comprises driver circuitry coupled at its outputs to said cables, and coupled at its inputs to said master sector PLL and said master clock generator, said driver circuitry adapted to boost signal levels. One would have been motivated to do so in order to provide drivers at the PLL for boosting low level signals, thereby improving the quality of signal transmission.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine Ng whose telephone number is (571) 272-3124. The examiner can normally be reached on M-F; 8:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C. Ng CN
May 11, 2007

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